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EXAMINER	
FAULK, DEVONA E	
ART UNIT	**PAPER NUMBER**
2644	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/657,833	SHUTTLEWORTH, TIMOTHY	
	Examiner	Art Unit	
	Devona E. Faulk	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1,3,4,9-16, 21,24,26, 28 and 31-34** are rejected under 35 U.S.C. 102(b) as being anticipated by Ferland et al. (U.S. Patent 5,883,523).

Regarding **claim 1**, Ferland discloses a testing system having a clock source (28) (Figure 1), which reads on "a clock"; a switching power supply (32) (Figure 1) that pulse width modulates a DC signal and then applies the pulse width modulated signal to the primary of a transformer (column 2, lines 7-15), which reads on "a pulse width modulated power processing device"; a digitizer (14) that samples the DUT (11) output signal (column 4, lines 30-36), which reads on a "digital signal processor". Note that the other components of the tester can also read on pulse width modulated power processing device since they are receive power from the switching power supply (column 4, lines 62-65). The digitizer and the switching power supply (32) are connected to the clock source (28) (Figure 1) and this reads on "wherein said pulse width modulated power processing device is communicatively coupled to said clock" and wherein said digital signal processor is coupled to said clock". The clock source (28) produces a reference clock signal ROSC that is used by all components of the system as a master timing reference (column 4, lines 16-36), which reads on "wherein said pulse width modulated power

processing device and said digital signal processor use said clock source for their operational clock frequencies".

All elements of **claims 3,9 and 13** are comprehended by claim 1.

Regarding **claim 4**, Ferland teaches that the power-processing device provides power that transmits power to all other components of the tester (10) (column 4, lines 62-66).
Claim 10 claims the system of claim 9 wherein the digital signal processor uses a multiple of the clock frequency for its operation. As stated above apropos of claim 9, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 10 with the exception of the claimed matter.

Regarding **claims 10, 11, and 12** Ferland discloses that the digitizer (14) uses integer multiples of the clock signal for sampling (Column 4, lines 27-36).

Regarding **claims 14-16,** Ferland discloses that the digitizer (14) uses integer multiples of the clock signal for sampling (Column 4, lines 27-36). Either of the components of the tester can also read on pulse width modulated power processing device since they are receive power from the switching power supply (column 4, lines 62-65).

Regarding **claim 21**, Ferland discloses a testing system having a clock source (28) that produces a reference clock signal ROSC that is used by all components of the system as a master timing reference (column 4, lines 16-36), (Figure 1); a switching power supply (32) (Figure 1) that pulse width modulates a DC signal and then applies the pulse width modulated signal to the primary of a transformer, which reads on "pulse width modulated power processing device; a digitizer (14) that samples the DUT (11) output signal (column 4, lines 30-36), which reads on a "digital signal processor". This all reads on "using the clock to operate a digital signal

processor (DSP)" and "using the clock to operate a pulse width modulated (PWM) power processing device". The method is inherent in the functionality of the system.

All elements of **claims 24, 31 and 32** are comprehended by claim 1.

Regarding **claim 26**, Ferland Figure 1 indicates that both the digitizer (14) and the switching power supply (32) each have an input and an output. All elements of claim 26 are comprehended by claim 21.

Regarding **claim 28,** Ferland teaches that the PWM power supply supplies power to all components of the tester (Column 4, lines 27-36).

Regarding **claims 33, 34** Ferland discloses that the digitizer (14) uses integer multiples of the clock signal for sampling (Column 4, lines 27-36). Either of the components of the tester can also read on pulse width modulated power processing device since they are receive power from the switching power supply (column 4, lines 62-65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 2,5,6,22,23,25, and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferland et al. (U. S. Patent 5,883,523) in view of Bryant (U.S. Patent 4,061,909)

Claim 2 claims the system of claim 1 wherein the power-processing device is a pulse width modulated power amplifier. As stated above apropos of claim 1, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 2 with the exception of the claimed matter. As stated above apropos of claim 1, all the components of the tester can read on the pulse width power-processing device since they all receive power from the switching power supply. Bryant teaches of a variable waveform synthesizer having current amplifiers (Figures 1 and 3). The current amplifier reads on power amplifier. Modifying Ferland's tester by using Bryant's concept of a variable waveform synthesizer reads on the claim language. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a digital switching amplifier as the power-processing device for the benefit of allowing selection between a variety of possible outputs.

Claim 5 claims the system of claim 3 wherein the power-processing device further includes a pulse width modulated power amplifier. As stated above apropos of claim 3 the combination of Ferland and Bryant meets all elements of that claim. Therefore, the combination meets all elements of claim 4 with the exception of the claimed matter. Bryant teaches of a variable waveform synthesizer having current amplifiers (Figures 1 and 3). The current amplifier reads on power amplifier. Modifying Ferland's tester by using Bryant's concept of a variable waveform synthesizer reads on the claim language. Either of the components of the tester can also read on pulse width modulated power processing device since they are receive power from the switching power supply (column 4, lines 62-65). Thus it would have been obvious one of ordinary skill in the art at the time of the invention to have the waveform synthesizer to include a power amplifier for the benefit of having the capability of producing

synthesized waveforms in response to signals or commands from the digital systems with whom it interfaces.

Claim 6 claims the system of claim 5 wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor. As stated above apropos of claim 5 the combination of Ferland and Bryant meets all elements of that claim. Therefore, the combination meets all elements of claim 6 with the exception of the claimed matter. Bryant teaches of a variable waveform synthesizer having current amplifiers (Figures 1 and 3). The current amplifier reads on power amplifier. Modifying Ferland's tester by using Bryant's concept of a variable waveform synthesizer reads on the claim language. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to power supply provide power for both the DSP and PWM amplifier for the benefit of mitigating the effects of power supply noise.

Claim 22 claims the method of claim 21, wherein the clock is within the DSP. As stated above apropos of claim 21, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 22 with the exception of the claimed matter. Although, Ferland does not disclose the clock being located internal to the digitizer (14), it does not make a difference if the clock were internal or external to the DSP because it will have the same functionality regardless. Thus it would have been obvious to have the clock internal to the digitizer for the benefit of having

Claim 23 claims the method of claim 21 wherein the PWM power-processing device is a PWM power amplifier. As stated above apropos of claim 1, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 2 with the exception of the claimed

matter. As stated above apropos of claim 1, all the components of the tester can read on the pulse width power-processing device since they all receive power from the switching power supply. Bryant teaches of a variable waveform synthesizer having current amplifiers (Figures 1 and 3). The current amplifier reads on power amplifier. Modifying Ferland's tester by using Bryant's concept of a variable waveform synthesizer reads on the claim language. The method is obvious in the functionality of the device. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a digital switching amplifier as the power-processing device for the benefit of allowing selection between a variety of possible outputs.

Claim 25 claims the method of claim 24, wherein the PWM power supply provides power to the DSP and to a PWM power amplifier. As stated above apropos of claim 24, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 25 with the exception of the claim matter. Ferland teaches of a PWM power supply that supplies power to all components of the tester. Bryant teaches of a variable waveform synthesizer having current amplifiers (Figures 1 and 3). The current amplifier reads on power amplifier. Modifying Ferland's tester by using Bryant's concept of a variable waveform synthesizer reads on the claim language. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to power supply provide power for both the DSP and PWM amplifier for the benefit of mitigating the effects of power supply noise.

Claim 30 claims the method of claim 23, wherein the PWM power amplifier drives a computer. As stated above apropos of claim 23 the combination of Ferland and Bryant meets all elements of that claim. Therefore, the combination meets all elements of claim 30 with the exception of the claimed matter. Ferland and Bryant discloses a waveform synthesizer with a

current amplifier (power amplifier) that drives the DUT. The DUT processes signals it receives. A computer is defined as a device that processes information. Therefore, all elements of claim 30 are comprehended by claim 23. Therefore, claim 30 is rejected for reasons given above in claim 23.

5. **Claims 17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Adrian et al. (U. S. Patent 5,617,058) in view of Ferland et al. (U.S. 5,883,523).

Regarding **claim 17**, Adrian teaches of a digital switching amplifier (Figure 10) comprising a switching power supply (56) and a digital signal processor (50) and a crystal timing reference (53) which reads on "a pulse width modulated power supply", "a pulse width modulated power amplifier" and "a digital signal processor" and "a clock". Adrian further teaches that the amplifier output and PWM scheme is determined by or controlled by the crystal timing reference (53) (column 13, lines 37-44). Although Adrian teaches on the above named elements, he fails to disclose the crystal timing reference controlling also the DSP and the power supply. However, the concept of a common clock controlling different elements of a system was well known in the art at the time of filing as taught by Ferland. Ferland discloses a circuit testing apparatus having a common clock (28) that supplies a master timing signal (ROSC) to a switching power supply (32) a digitizer (14) and a waveform synthesizer (12). Although, Adrian does not disclose the crystal timing reference being located internal to the digital signal processor (50), it does not make a difference if the crystal timing reference where internal or external to the DSP because it will have the same functionality regardless. Figure 10 indicates that all elements are connected. Using Ferland's concept of a common clock would read on "wherein said pulse width modulated power supply is communicatively coupled to said clock in

said digital signal processor ", "wherein said pulse width modulated power supply is communicatively coupled to said clock in said digital signal processor" and " wherein said digital signal processor and said pulse width modulated power supply and said pulse width modulated power amplifier use said clock in said digital signal processor for its operational clock frequency". Thus it would have been obvious to one of ordinary skill in the art to modify Adrian's digital switching amplifier by using Ferland's concept of a common clock for the benefit of producing synchronized data.

Claim 18 claims the system of claim 17, wherein the pulse width modulated power supply provides power to the pulse width modulated power amplifier and the digital signal processor. As stated above apropos of claim 17 the combination of Adrian and Ferland meets all elements of that claim. Therefore, the combination meets all elements of claim 18 with the exception of the claimed matter. Ferland teaches of a pulse width modulated power supply providing power to the digital signal processor and to the other components of the tester. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Adrian's device by using Ferland's concept of the power supply providing power to the digital signal processor and amplifier for the benefit mitigating the effects of power supply noise.

Claim 19 claims the system of claim 17 wherein the digital signal processor operates at 96 kHz. As stated above apropos of claim 17 the combination of Adrian and Ferland meets all elements of that claim. Therefore, the combination meets all elements of claim 18 with the exception of the claimed matter.

Claim 20 claims the system of claim 17 wherein the pulse width modulated power amplifier drives a speaker. As stated above apropos of claim 17 the combination of Adrian and

Ferland meets all elements of that claim. Therefore, the combination meets all elements of claim 20 with the exception of the claimed matter. Adrian teaches that the amplifier drives speaker (60) (Figure 10, column 17, lines 27-29). All elements of claim 20 are interpreted by claim 17. Therefore, claim 20 is rejected for reasons given above in claim 17.

6. **Claims 7 and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferland et al. (U.S. 5,883,523) in view of Abe et al. (U. S. Patent 4,173,790)

Claim 7 claims the system of claim 1, wherein the clock operates at 96 kHz. As stated above apropos of claim 1, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 7 with the exception of the claimed matter. Ferland does not teach of the clock operating frequency. Abe teaches of a clock generator operating at 96 kHz (column 8, lines 35-41). It is well known in the art that clocks can operate at a range of frequencies and it would be a matter of design choice as to the frequency. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have Ferland's clock operating at 96 kHz for the benefit of meeting a design specification.

Claim 35 claims the system of claim 21, wherein the clock operates at 96 kHz. As stated above apropos of claim 21, Ferland meets all elements of that claim. Therefore, Ferland meets all elements of claim 35 with the exception of the claimed matter. Abe teaches of a clock generator operating at 96 kHz (column 8, lines 35-41). It is well known in the art that clocks can operate at a range of frequencies and it would be a matter of design choice as to the frequency. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have Ferland's clock operating at 96 kHz for the benefit of meeting a design specification.

7. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Adrian et al. (U. S. Patent 5,617,058) in view of Ferland et al. (U.S. 5,883,523) in view of Abe et al. (U. S. Patent 4,173,790).

Claim 19 claims the system of claim 17 wherein the clock in said digital signal processor operates at 96 kHz. As stated above apropos of claim 17, the combination of Adrian and Ferland meets all elements of that claim. Therefore, the combination meets all elements of claim 19 with exception of the claimed matter. Ferland teaches of a clock that is the master timer for the components in the system. Abe teaches of a clock generator operating at 96 kHz (column 8, lines 35-41). It is well known in the art that clocks can operate at a range of frequencies and it would be a matter of design choice as to the frequency. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have Adrian and Ferland's clock operating at 96 kHz for the benefit of meeting a design specification.

8. **Claims 8 and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferland et al. (U. S. Patent 5,883,523) in view of Bryant (U.S. Patent 4,061,909) in further view of Adrian (U. S. Patent 5,617,058)

Claim 8 claims the system according to claim 5, wherein the pulse width modulated power amplifier drives a loudspeaker. As stated above apropos of claim 5 the combination of Ferland and Bryant meets all elements of that claim. Therefore, the combination meets all elements of claim 8 with the exception of the claimed matter. Adrian teaches of a power amplifier that drives a loudspeaker. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have the DUT be a speaker driven by Adrian's amplifier for the benefit of testing a loudspeaker.

Claim 29 claims the system according to claim 23, wherein the pulse width modulated power amplifier drives a loudspeaker. As stated above apropos of claim 23 the combination of Ferland and Bryant meets all elements of that claim. Therefore, the combination meets all elements of claim 29 with the exception of the claimed matter. Adrian teaches of a power amplifier that drives a loudspeaker. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have the DUT be a speaker driven by Adrian's amplifier for the benefit of testing a loudspeaker.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 703-305-4359. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Devona Faulk

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PRIMARY EXAMINER